A CCTV Image Grabber for Vehicular Parameter Detection.

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Abstract

The concept of vision information has become a key feature in modern vehicular traffic control and *Intelligent Vehicle Highway Systems* (**IVHS**) [1]. Vehicle detection by video cameras is one of the most promising new technologies used in implementing advanced traffic control and management systems [2].

The CCTV Image Grabber discussed in this paper is a low cost design which can capture, store and transmit video information to a remote computer for visual site inspection and extraction of vehicular traffic parameters for adaptive control of road traffic.

1. Introduction.

As the problem of urban traffic congestion spreads, there is a pressing need for the introduction of advanced technology and equipment to improve the state of the art of traffic control [2]. In this context, the techniques used for sensing traffic flow information plays a vital role in ensuring accurate real time controllability.

The techniques such as inductive loops & pressure tubes are becoming obsolete now due to limitations in measuring some important traffic parameters and accurately assessing traffic conditions. These types of detectors do not have visual surveillance capabilities and their placement is not flexible too. (i.e. detect traffic only at fixed points.) Only the presence or absence of vehicles focused on to the detectors can be accessed [2].

The required traffic parameters such as vehicle speed, queue length and traffic composition can only be derived by multi-point detection schemes [2]. This concept entails detection of vehicles and extraction of traffic parameters in real time from images generated by video cameras overlooking a traffic scene.

Closed Circuit television (CCTV) has gained popularity because of its ability to provide diverse information on relatively large regions leading to opportunities for performing substantially more complex tasks than conventional detection schemes. A single camera can replace many detection loops providing a true wide area detection with cost effectiveness. [1][2]

By processing these video images, traffic parameters such as speed, traffic composition, queue length etc. can be extracted. In addition CCTV images can be further processed for extraction of other useful information such as detection of vehicle shapes and types, occurrence of traffic violations and vehicle identification numbers etc.

To introduce CCTV based vehicle detection for automation of road traffic control in Sri Lanka involves an ill-affordable investment to purchase foreign technology and equipment unless some locally developed system is introduced. The CCTV Image Grabber discussed in this paper is as a result of research carried out at the *Department of Electronic and Telecommunication Engineering, University of Moratuwa* in collaboration with *Road Construction and Development Company* (**RC&DC**), Sri Lanka. The image grabber is meant for capturing, storing and transmitting video information to be used in traffic control systems, at a much reduced cost.

2. Design requirements and limitations.

The Image Grabber described in this paper is meant for producing digitized video data for extraction of vehicular parameters. In this context, the design has to cater for an acceptable image resolution (i.e. both pixel and grey scale resolution.) with real time operation as applied to vehicular traffic control. Also the design cost has to be affordable such that it can actually be applied for automation of road traffic control and management in Sri Lanka, using a fairly low budget.

The design requirements could be easily satisfied by employing a general purpose video capturing board available in the market. But, due to the very high cost the use of such boards is not feasible. Therefore a low cost video capturing board has been designed to meet the specific requirements.

It basically requires two closely spaced image frames for extraction of vehicular parameters corresponding to a particular time. To cater for this requirements, the Image Grabber has to store two image frames in a fast accessible Random Access Memory simultaneously. Also the system has to incorporate the facility for selecting the time duration between the two stored image frames.

Processing for extraction of traffic parameters can be done either at the detection site itself or at the central traffic controller located remotely. In the first case, the traffic parameters after being extracted locally need to be transmitted to the central traffic controller whereas in the latter case the complete image is to be transmitted to the remote site for processing. In both cases the most economically viable transmission means is through the telephone lines as provided by the existing infrastructure in Sri Lanka.

In the case of complete image transmission, visual inspection of the traffic scene is also possible at the remote site in addition to machine based vehicular traffic parameter extraction. This feature becomes very attractive in verifying the functionality of the traffic control system especially at the initial development stage.

To support the real time controllability of the traffic control system, the image frame rate allowable through telephone lines is quite sufficient. This is because, according to the sequence control algorithms, a change of parameters are required after several minutes from the previous change.

If a DSP processor is employed at the detection sight, it can be used to compress image information in addition to extraction of traffic parameters. This creates a lower processing load on the central traffic controller, allowing it spare time to carry out other traffic control and management functions effectively. Also the visual inspection feature can be made more attractive with a higher image frame transfer rate, made possible by image compression. This technique also allows several video inputs to share the same digitizing hardware and the same transmission medium in a time-multiplexed manner.

The resulting advantages due to a DSP processor are to be gained at the expense of its high cost. Therefore this initiative step in introducing CCTV for automated traffic control in Sri Lanka, within a low budget scope, will leave the use of a DSP processor as a future development idea.

3. System Performance.

The CCTV image grabber captures grey scale video information in real time from a monochrome or colour video signal. The system input can be either interlaced or non-interlaced with field repetition frequency 50Hz or 60 Hz. A field of the video signal is stored as a 256*256 digital image matrix with 8-bit grey scale resolution. In the system RAM two such fields can be stored simultaneously where inter-field separation can be programmed. The stored information can be transmitted to the remote Central Traffic Controller, via a telephone link, for further processing.

The system can transmit video information at nearly 2 frames per minute. Hence the detection parameters can be updated at a maximum rate of one update per minute. Also the traffic scene can be visually displayed on a monitor with a refresh frame once in every 30 seconds. Apart from this four video channel inputs can be multiplexed as selected by the remote PC.

4. System Architecture.

The Overall system architecture of the CCTV image Grabber is depicted in fig 1. It consists of five modular sub systems, *Sensor Interface Unit* **(SIU)**, *Digitizing and Storage Unit* **(DSU)**, *Microprocessor Unit* **(MPU)**, *Transmission Unit* **(TXU)** and *Power supply Unit* **(PSU)**.

4.1. Sensor Interface Unit (SIU).

Basically this comprises an analog multiplexer which selects one out of *a maximum of 4 video channel inputs* for digitization. Selection controls for the multiplexer is applied via a register latch accessed by MPU.

4.2. Microprocessor Unit (MPU).

The Z-80 based MPU is used as the interface between DSU and the modem. The MPU generates capturing parameters to DSU and SIU and dumps storage information to the remote PC.

The system architecture of the Z-80 MPU is depicted in fig.2. The Z-80 operates at a clock speed of 4Mhz. The MPU constitutes Z-80 CPU, CTC, DART, RAM, EPROM, line drivers and other required buffers and logic Ics [3] [4].

The MPU interfaces DSU via four output latches and one input buffer, which will be discussed in detail under the description of DSU. It interfaces the telephone link through a modem.

4.3. Digitizing and Storage Unit (DSU).

Fig 3. Depicts the architecture of the Digitizing and Storage Unit **(DSU)**. The Z-80 MPU accesses DSU via four latches and one input buffer. The *control latch* commands the *control Unit* of DSU. The *offset latch* sets the offset of the video input applied to the A/D converter. The *gain control latch* sets the gain of the video amplifier. The *video channel selection latch* sets the analog multiplexer to select the required video channel to the DSU. Storage RAM is accessed by the MPU via the input buffer.

4.4. Control Unit.

This comprises an FSM and other logic sections. MPU instructs the CU via the *control latch*, which is an 8 bit register with following bit definitions.

1. M_0 mode control
2. M_1 mode control
3. Capture   Start of capturing
4. X_clock   X-address counter clock s
5. Y_clock   Y-address counter clock s
6. Bank Select   to switch between RAM banks
7. Not used
8. Not used

4.4.1. Finite State Machine (FSM).

The hard wired FSM takes over the control of the image grabber in *Capture Mode* (**MODE_C**) by properly sequencing the capturing process. This operates at a clock speed of 4MHz, digitizing and storing picture information in the SRAM.

The state transition diagram of the FSM is illustrated in fig 4. The FSM is not activated until MODE_C is selected and *start of capturing* signal is given by the MPU. With that, detecting the first occurrence of Vertical Blanking period the FSM changes state from S_0 to S_1. At state S_1 the first field is stored in the lower bank of the SRAM. The end of field is recognized by detecting the address counter overflow status when 32KB address space is completed. On completion of the first field the FSM moves to state S_2 and wait until the MPU instructs to capture the next field and when instructed FSM changes state from S_2 to S_3 and waits for the occurrence of the immediate V_Blank signal. With that at state S_4 the second field is stored in the upper-half of the SRAM. Ultimately the FSM rests at state S_5 until the mode is changed or the next capturing signal is issued.

4.5. Transmission Unit (TXU).

This constitutes two modems at either side of the telephone line. The modems are connected to the MPU at the capturing end and to a PC at the remote end.

4.6. Power Supply Unit (PSU).

Generates power for all modules. Outputs +5v,-5V for DSU; +5V for MPU, +12V, -12V for line drivers .

5. Principle of Operation.

The system operates in three functional modes, the *Stand by Mode* (**MODE_S**), the *Capture Mode* (**MODE_C**) and the *Transmission Mode* (**MODE_T**). In MODE_S the DSU goes to tri-state disabling RAM access and other buffers and latches. In MODE_C the system operates entirely under hardwired control in order to cater for high speed capturing process, required for real time operation. In MODE_T control is taken by the Z-80 microprocessor unit to dump the stored video information to a destination PC via a telephone link.

The remote PC can request the local Z-80 MPU to start capturing with specified parameters. (field separation, video channel selection, video signal offset and gain of the video amplifier, inter-field separation etc.) When the request is made the Z-80 MPU loads the appropriate control registers with specified values and triggers MODE_C operation transferring the

control to a FSM based hard wired logic. In a single capturing cycle, where a field is stored as a 256*256 image matrix with 8 bit grey scale resolution, two fields with a given field separation can be captured. On a dump request the stored video information is transmitted to the remote PC under the control of Z-80 MPU.

5.1. Capturing Parameters.

Two fields of video information are stored in the RAM for one capturing cycle with following parameter settings.

- 256 rows per field.
- 256 samples per row.
- 8 bit grey scale resolution per sample.
- Inter field duration programmable by the remote PC.
- Multiplexing capability for 4 video input channels.

Under these requirements the video signal is digitized at a rate of 4Msamples per second. In addition, the video input to the A/D converter can be optimized by varying offset and gain parameters of the video amplifier on software request.

5.2. Storage RAM.

Four TC55257DPI SRAM chips forming a 128 KB high speed RAM bank [5] is used to store the two fields of video information. The first field is stored in the lower (64KB) half of the SRAM bank whereas the other field is stored in the upper (64KB) half of the SRAM bank. A field is stored in 256 segments of the SRAM where in each segment of 256 bytes a row is stored. Thus an image with 256 rows at 256 bytes per row is stored as a field. Two such fields can be stored simultaneously in one scan.

In the capturing mode the X-counter progressively scans the image along a row with 4MHz system clock. The Horizontal Sync (H-sync) is used as the clock for the Y-counter which sets the higher address byte of the RAM address storing each row in respective segments. A FSM generated signal is used to select lower and upper banks for the tow fields. The control signals issued for the SRAM are depicted in fig.3.

Thus a field is stored as a 256*256 matrix image in the SRAM with the row number as the segment index addressed by the higher byte of the SRAM address. So in Transfer Mode (Mode_T) a stored field can be directly read in blocks of 256 Bytes with MPU generated X-clock and Y-clock signals.

6. Offset/Gain controllability of the of the video amplifier.

TDA 8703 high speed (40MHz) A/D converter is used for digitizing the signal. For its full scale operation the input to the A/D converter has to be in the range 1.55V - 3.26V. Depending on the Contrast and brightness of the image the offset and gain settings of the video amplifier has to be changed adaptively in order to provide an optimal input to the A/D converter.

With changes in the ambient light conditions brightness of the image changes. This causes the video input to the A/D to shift from the valid input range, deteriorating the digitized image. This problem is addressed by implementing a mechanism by which the gain and the offset settings of the video amplifier are remotely manipulated. Thus the video input can be adaptively changed according to changes in ambient light conditions and can be made to lie

in the valid range. The design supports this facility with 256 offset levels and 256 gain values.

7. Conclusion.

The system described in this paper is a cost-effective design, to be adapted in automation of traffic control and management in Sri Lanka. At the initial stage of Automation of Road Traffic in Sri Lanka the system performance is quite satisfactory. Yet the system needs further improvements to meet the requirements of real sophisticated Traffic Control Systems. This creates a challenging research opportunity to design an enhanced product as the second stage of this research project.

Acknowledgment

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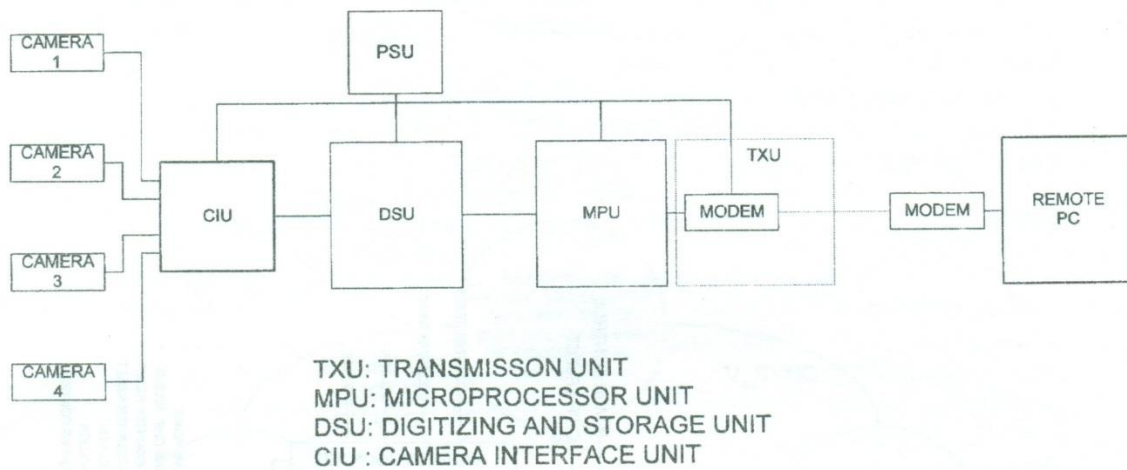[5]. Johnson JH, "Build Your Own Data Acquisition and Display Devices", McGraw-Hill, 1994.

CAMERA 1

CAMERA 2

CAMERA 3

CAMERA 4

PSU

CIU

DSU

MPU

TXU

MODEM

MODEM

REMOTE PC

TXU: TRANSMISSON UNIT
MPU: MICROPROCESSOR UNIT
DSU: DIGITIZING AND STORAGE UNIT
CIU : CAMERA INTERFACE UNIT

FIG. 1. THE SYSTEM ARCHITECTURE

CLOCK 4 MHz

RAM

Z-80 CPU

EPROM

REGISTERS AND BUFFERS

(INTERFACE TO DSU & CIU)

CTC

DART

+

LINE DRIVERS

PSU

FIG 2. MPU ARCHTECTURE

VIDEO
INPUTS

ANALOG
MULTIPLEXER

SYNC
SEPERATION

H-SYNC

V-SYNC

RDWR CONTROL

CHIP SELECT

Y-COUNTER RESET

X-COUNTER RESET

Y-CLOCK

X-CLOCK

ADDRESS COUNTER

RAM

BUFFER1   BUFFER2

VIDEO
AMPLIFIER
WITH
ADJUSTABLE
GAIN & OFFSET

A/D
CONVERTER

H-SYNC

V-SYNC

CLK

RAM RDWR

RAM CHIP SELECT

Y-COUNTER RESET

X-COUNTER RESET

Y-CLOCK

X-CLOCK

BUFFER CONTROL

CONTROL
UNIT
(CU)

(FSM AND OTHER
CONTROL LOGIC)

VIDEO CHANNEL
SELECTION
LATCH

OFFSET
CONTROL
LATCH

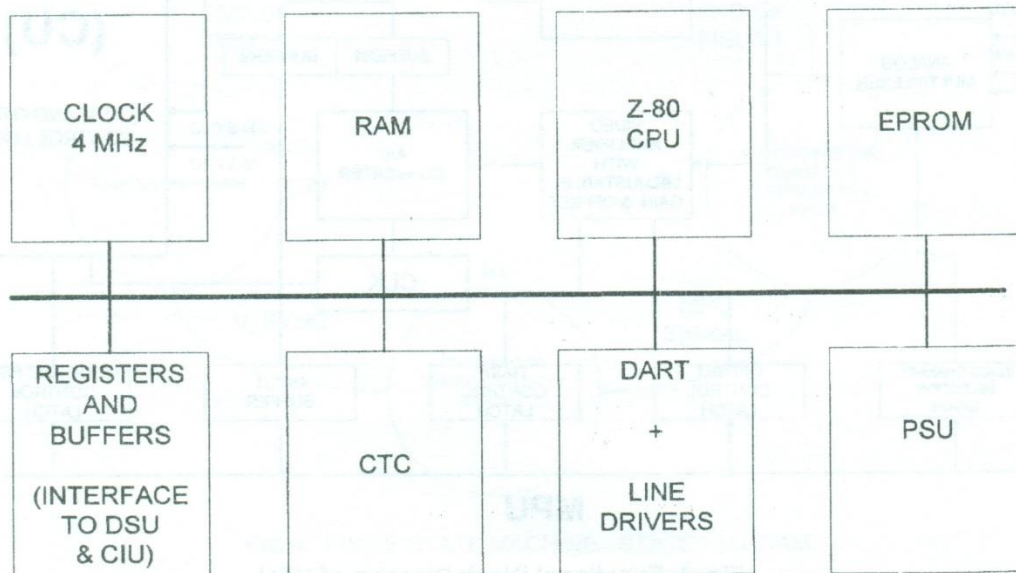GAIN
CONTROL
LATCH

INPUT
BUFFER
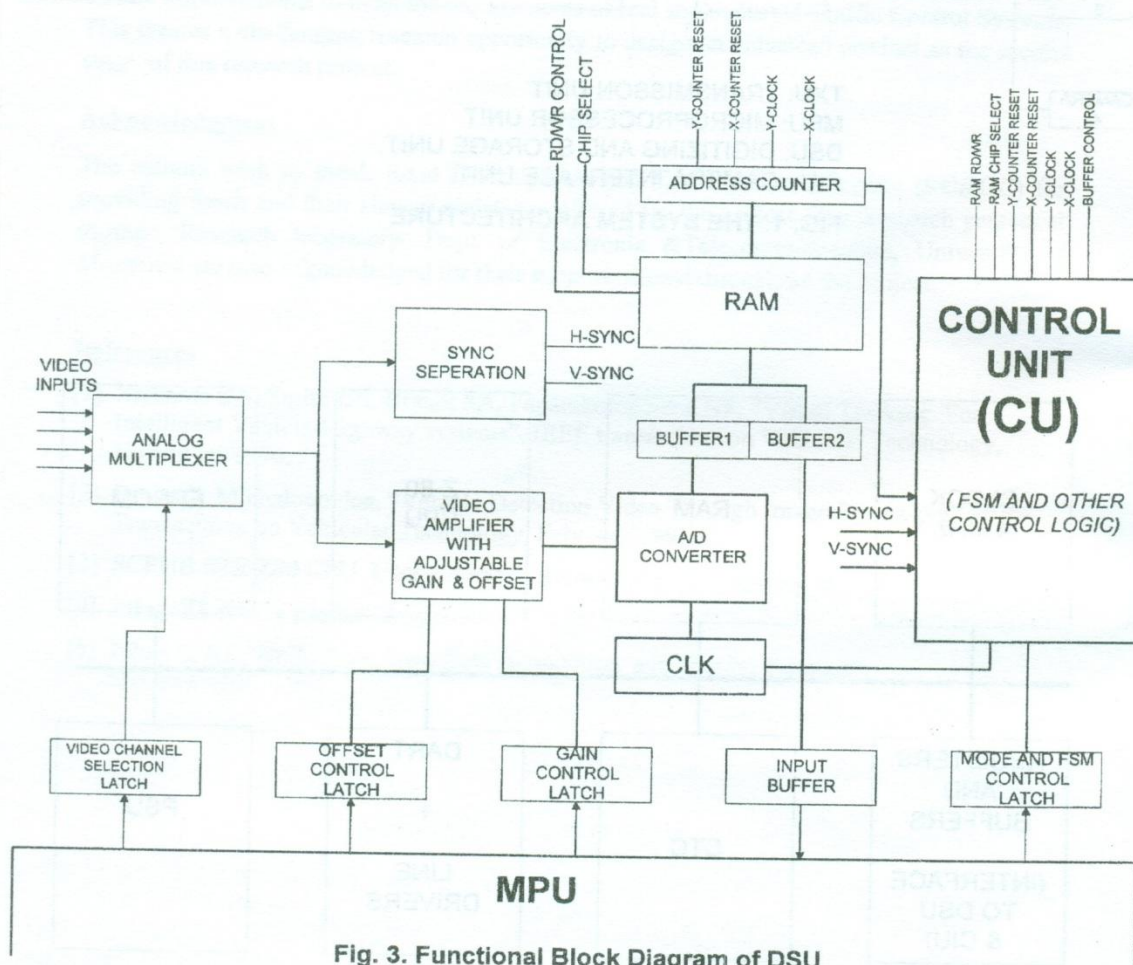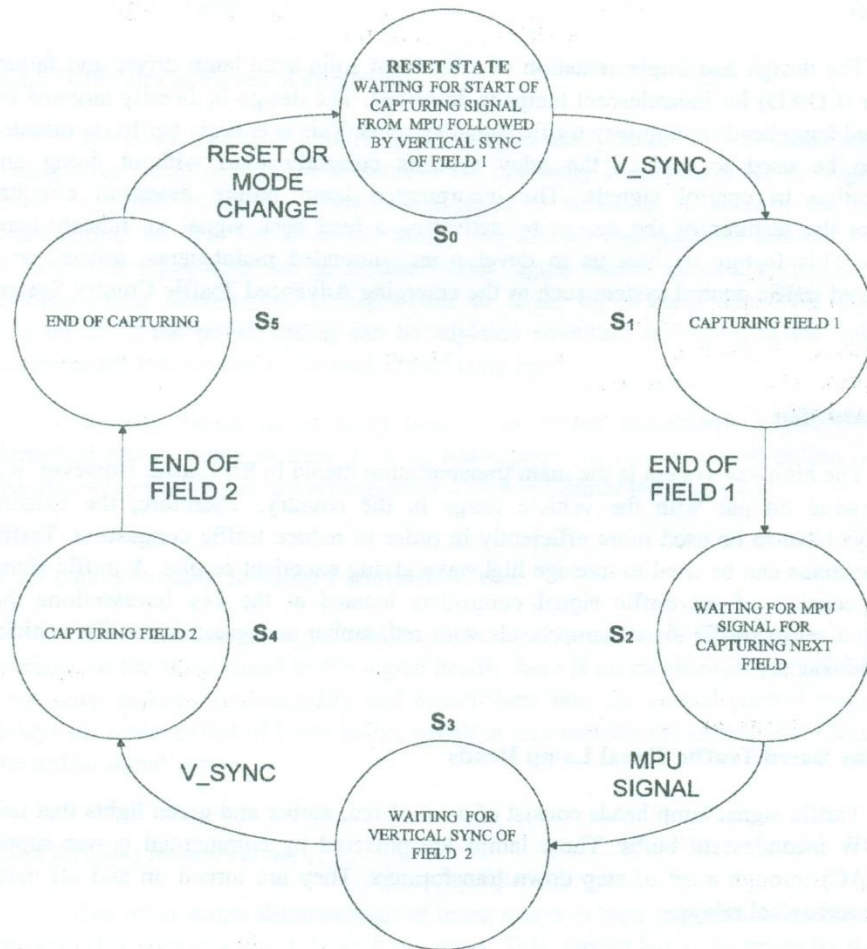
MODE AND FSM
CONTROL
LATCH

MPU

Fig. 3. Functional Block Diagram of DSU

FIG.4. FINITE STATE MACHINE - STATE DIAGRAM